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Electronic Conductivity and Dielectric Properties of Nanocrystalline CeO_2 Films

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Abstract. The growth of dielectric layers on silicon substrates has attracted a great deal of recent interest given their potential applicability in the fabrication of high quality silicon-on-insulator (SOI) structures, high density capacitor devices, and stable buffer layers between silicon and other materials. In this study, nanocrystalline CeO_2 films were deposited on n-type (100) silicon substrates using pulsed laser deposition (PLD) to form a gate dielectric for a Pt/n-Si/CeO_2/Pt MOS device. XRD, AFM and FESEM measurements were used to characterize the crystal structure and grain size of the CeO_2 films. The electrical properties of the device structure were examined by capacitance-voltage (C-V) and impedance spectroscopy measurements. The CeO_2 films exhibited an activated conductivity, characterized by an activation energy $E_a = 0.45$ eV. An estimated room temperature electron mobility μ_e of 2.8×10^{-7} cm^2/Vs leads to a corresponding electron concentration n of 5.5×10^{17} cm^{-3}. In contrast to conventional MOS capacitors, we find an additional capacitive contribution under strong accumulation conditions as a result of space charge effects inside the CeO_2 thin film.

Keywords: CeO_2, nanoparticles, MOS device, space charge effects

1. Introduction

Stable chemical properties, compatibility with silicon, ease of processing, high oxygen diffusivity and high dielectric constant make CeO_2 attractive as an electrolyte material for integrated solid oxide fuel cells (SOFC), gate dielectrics for MOS devices, and buffer layers between silicon and other functional ceramics, such as $PbTiO_3$ and $Pb(Zr,Ti)O_3$. Cerium dioxide (CeO_2) appears to be a particularly attractive candidate, given its high dielectric constant ($\varepsilon_r \approx 25$) and its compatibility with Si. In the solid state ionics arena, there is much interest in reducing the operating temperatures of solid state oxide fuel cells (SOFC) by shifting from bulk to thin film electrolytes (stabilized ZrO_2 or acceptor doped CeO_2) [1, 2]. The lattice constant mismatch between diamond-structured silicon and fluorite-structured CeO_2 is only about 0.35%, thus enabling the fabrication and deposition of stress free, highly oriented or epitaxial thin film structures. Furthermore, CeO_2 forms no undesirable reaction products, such as silicides, when in contact with silicon at elevated temperatures [3]. In this paper we describe the fabrication and characterization of the Pt/n-Si/CeO_2/Pt MOS device structure. The properties of the CeO_2 thin films are deconvoluted from the overall response of the MOS device with the assistance of impedance spectroscopy. The electrical properties of CeO_2 films are discussed in the context of the model describing the size effect caused by impurity segregation in grain boundaries that subsequently, decreases the overall resistivity of the nanocrystalline films [4].

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2. Experimental

CeO_2 thin films were deposited onto n-type silicon wafers by a pulsed KrF excimer laser (Lambda Physik

LPX-300) operating at a wavelength of 248 nm. The laser pulse energy was 400 mJ, with the beam fluence set to 3.65 J/cm^2 with aid of focusing optics. *In situ* deposition was carried out in a vacuum chamber at a temperature of 600°C with oxygen pressures 3.4×10^{-5} and 1.5×10^{-3} Torr, respectively. N-type silicon substrates with resistivity of 2–4 Ω cm and (100) surface orientation were placed parallel to the target at a distance of 65 mm from the target surface. Before deposition, the silicon substrates were etched with 5% HF in water and rinsed with deionized water. Both back and top platinum electrodes with thickness of 150 nm, and area of 130×10^{-6} and 2.40×10^{-6} m^2, respectively, were deposited by room temperature DC sputtering. A CeO_2 ceramic pellet, isostatically pressed at 290 MPa and afterwards sintered at 1425°C was used as a target. X-ray diffraction measurements (Rigaku RU300) were performed on both CeO_2 films and target. A tapping mode AFM (Nanoscope IIIa) and FESEM (JEOL JSM-6400) were used for the evaluation of thin film surface quality and microstructure. An impedance analyzer, with frequency sweep from 0.1 Hz to 1 MHz (Solartron 1260), was used for the electrical characterization of the MOS structure at temperatures from room temperature to 350°C. Impedance response of the Pt electrodes was measured from otherwise similar Pt/*n*-Si/Pt reference samples without CeO_2 film. At room temperature, resistance was below 1.5 kΩ and at elevated temperatures above 150°C resistance was less than 100 Ω, thus negligible compared to CeO_2 film resistance.

3. Results and Discussion

The crystal structure of the CeO_2 films was studied using XRD. Films deposited at a pressure of 3.4×10^{-5} Torr show a high intensity of around 20000 cps and strong orientation with the (111) planes parallel to the film surface. On the other hand, films deposited at a pressure of 1.5×10^{-3} Torr gave a low intensity and practically random orientation together with a background indicating the presence of an amorphous phase. From FESEM and AFM microstructure analysis it was found that both types of films were similar and consisted of grains with diameter typically 40–50 nm in diameter, except that the highly oriented film included also bigger crystals up to 100 nm diameter. Furthermore, a clear columnar structure of randomly oriented film with grain boundaries reaching through the film was revealed. In the case of nanocrystalline CeO_2 thin films, with thickness of $t_f \approx 75$ nm, the films are considered to consist of parallel sets of grains and grain boundaries reaching through the film.

In Fig. 1, the C-V response of the MOS device on *n*-Si, with randomly oriented columnar CeO_2 film, is

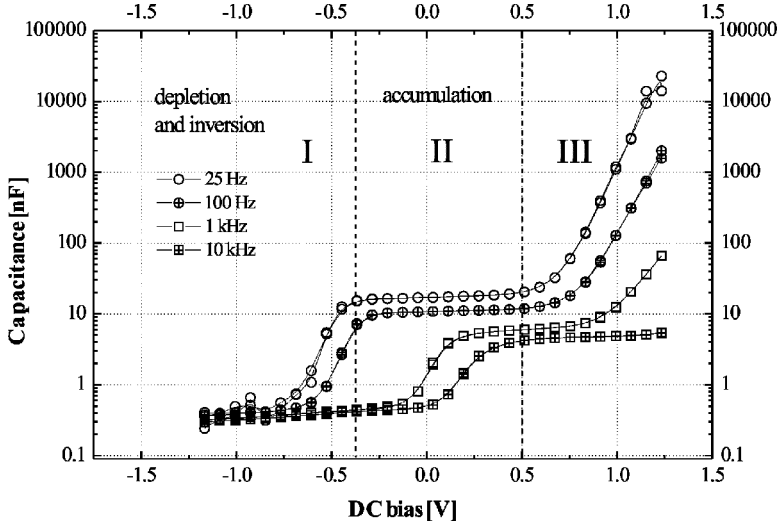

Fig. 1. Four C-V curves of a Pt/*n*-Si(100)/CeO_2/Pt device calculated from impedance spectroscopy data measured at 25 Hz, 100 Hz, 1 kHz, and 100 kHz. The span of the gate bias potential V_b is divided into the three regions **I**, **II**, and **III**, respectively.

shown plotted at a number of frequencies. The data are roughly divided into three regions, labeled **I**, **II**, and **III**, respectively, according to the applied gate bias voltage. The value of the oxide capacitance C_{ox} could be determined from the plateau in region **II**. There is a clear contribution of interface traps at the n-Si/CeO_2 and Pt/n-Si interfaces inducing a shift of the flat band voltage of the device from the ideal high frequency value of $V_{FB} \approx 0.6$ V. More interestingly, also the value of the capacitance C_{ox} was found to depend on the measurement frequency. In region **III**, the C-V response starts to increase again as a function of increasing gate potential. This behavior of nonsaturated capacitance under strong accumulation was also reported by Sakai et al. [5]. The dielectric constant ε_r, as determined from the capacitance $C_{ox} \approx 5$–15 nF plateaus in region **II** of Fig. 1, is plotted as a function of frequency in Fig. 2. The value $\varepsilon_r \approx 22$ was selected to represent the dielectric constant of thin film CeO_2, although the value increased with decreasing frequency below 100 Hz. The loss angle, with absorption peak around 100 Hz, was determined from the impedance spectroscopy measurements as $\tan\delta = Z''/Z'$. This type of loss angle behavior is typically related to space charge polarization in heterogeneous materials [6]. Since the nanocrystalline

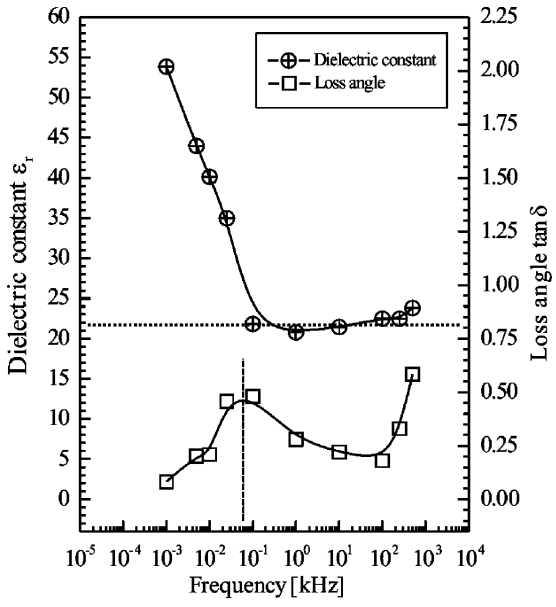

Fig. 2. Dielectric constant ε_r and loss angle $\tan\delta$ as a function of frequency of randomly oriented columnar CeO_2 film under the biasing condition of region **II**.

CeO_2 thin films studied here were assumed to consist of columnar grains reaching through the film, the theory of heterogeneous space charge polarization is hardly applicable due to the missing grain boundaries perpendicular to the applied electric field. However, since the room temperature mobility of CeO_2 is very low, there remains the possibility of charge concentration fluctuations at low frequency electric fields, leading to space charge effect polarization. Also, the increased electron concentration screens the Coulomb potentials of the positive defects, e.g., oxygen vacancies $V_O^{\cdot\cdot}$, by changing the local charge distribution and so altering the overall dielectric function [7].

The conductivity of the CeO_2 films was determined from the impedance spectroscopy arcs at several temperatures using conventional RC-circuit fitting procedure. In Fig. 3(a), the temperature response of both the highly oriented sample with an activation energy of $E_a = 0.44$ eV, and the columnar film with $E_a = 0.45$ eV is shown. Data in Fig. 3(a) was collected by using a *dc*-bias of $V_b = 0$ V and *ac*-signal amplitude of 20 mV thus presetting the component into region **II**, as determined from Fig. 1. The electronic conductivity of the columnar film was found to be about three orders of magnitude higher than that of oriented film, but still controlled by the small polaron hopping bulk conductivity. Enhanced electron generation in nanocrystalline CeO_2, first reported by Chiang et al. [4] is attributed to the formation of a positive grain boundary charge induced by segregation of cation impurities to the grain boundaries [8, 9]. The concentration of excess electrons, induced in the corresponding negative space charge regions bordering the grain boundaries, increases drastically in nanocrystalline CeO_2 given the large volume fraction of grain boundaries. This is most likely the reason for the higher conductivity of the columnar film given its smaller grain size and larger density of grain boundaries as compared to the more highly oriented film with columnar grains. The room temperature conductivity of $\sigma = 2.467 \times 10^{-8}$ S/cm corresponds to an electron concentration of $n = 5.5 \times 10^{17}$ cm^{-3}. The concentration n was calculated using measured conductivity σ and estimated value of mobility $\mu_e = 2.8\times 10^{-7}$ cm^2/Vs based on known dependence of CeO_2 stoichiometry and mobility μ_e on the measured activation energy $E_a = 0.45$ eV [10]. Conductivity of MOS device with columnar CeO_2 film under *dc*-bias of $V_b = 1.0$ V presetting the component into region **III** is presented in Fig. 3(b). Now the simple response of unbiased component has split into

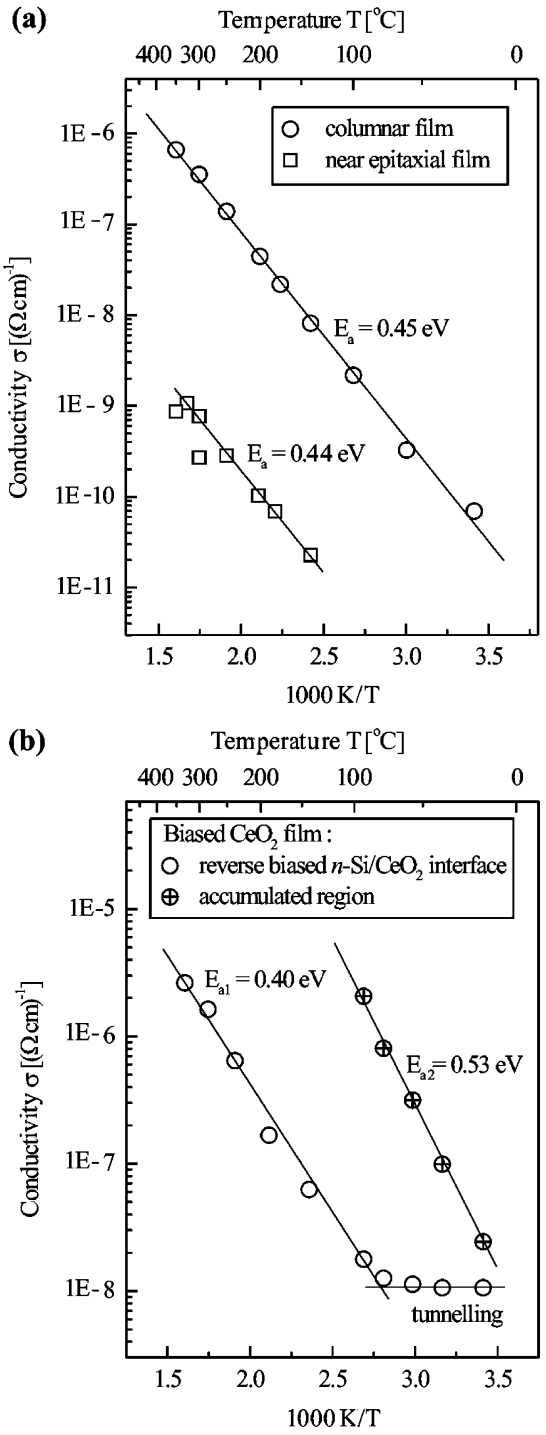

Fig. 3. Conductivity of CeO_2 films in the Pt/n-Si/CeO_2/Pt MOS structure as a function of temperature. (a) Columnar (○) and highly oriented epitaxial (□) films under the biasing condition of region **II**. (b) Columnar film under the biasing condition of region **III** with $V_b = 1.0$ V.

two contributions with $E_a = 0.40$ eV and tunnelling, and $E_a = 0.53$ eV, respectively. Observed tunnelling effect is assumed to appear through a depletion region w generated by the excess bias V_b in CeO_2 film.

In Fig. 1, the region **III** deserves some further consideration. Since the smallest capacitance connected in series dominates the total capacitance, there has to be an alteration in oxide capacitance C_{ox} in region **III**. Under *dc*-bias conditions and at low frequencies below the loss angle absorption peak around 100 Hz, the increase of the capacitance is clearly due to space charge limited leakage conduction (SCLC). However, if one considers such a high electron concentration with low mobility and conductivity, the space charge polarization effects due to the depletion of CeO_2 at low frequencies are possibly the dominant phenomena controlling the observed C-V response. Once the excess bias starts to deplete the oxide film, beginning from the n-Si/CeO_2 interface, the accumulated part of the CeO_2 grains ($t_f - w$) acts as a space charge region giving rise to the measured capacitance, and the total capacitance C_{tot} of the device can be described by the formula:

$$\frac{1}{C_{\text{tot}}} = \frac{1}{C_w} + \frac{1}{C_{t_f - w}} = \frac{1}{\varepsilon_0 A}\left[\frac{w}{\varepsilon_r} + \frac{t_f - w}{\varepsilon_r^*}\right], \quad (1)$$

where t_f is the film thickness, A is the gate electrode area, w is the width of the depletion layer in n-Si/CeO_2 interface, and ε_r^* is the effective dielectric constant of accumulated part of the film. At the beginning of the depletion process, the depletion layer capacitance C_w is much bigger than the accumulation capacitance $C_{t_f - w}$ and thus the latter dominates. Since w saturates eventually with increasing gate potential V_b, the capacitance C_w will attain a minimum value, as was found in our previous studies [11]. Clearly, if $\varepsilon_r^* = \varepsilon_r$, Eq. (1) gives the relation $1/C_{tot} = 1/C_{ox}$. This is most likely the case at high frequencies of 10 kHz and above where slowly moving space charge freezes out. This kind of behavior, with bias-dependent accumulation capacitance, is typical in complex semiconductor heterostructures applied in photonic devices [12]. Once the depletion layer w in CeO_2 film is formed, it is possible to explain the conductivity properties shown in Fig. 3(b). The curve with activation energy $E_{a1} = 0.40$ eV and tunneling current response at lower temperatures now represent the conductivity of the depletion layer in the CeO_2 film with w ($V_b = 1.0$ V). At temperatures above 90°C, the Schottky emission over the potential barrier at the n-Si/CeO_2 interface dominates. The

work function difference for the doped Si substrate and CeO_2 film materials is $\phi_{CeO_2} - \phi_{n-Si} = (4.69 - 4.30)$ eV $= 0.39$ eV. The other curve with activation energy $E_{a2} = 0.53$ eV represents the conductivity of the accumulated part $(t_f - w)$ of the CeO_2 film. The conductivity increased by more than one order of magnitude due to the rise of the electron concentration and screening of the Coulomb trap potentials of the oxygen vacancies [13]. The rise of the activation energy from $E_a = 0.45$ eV to E_{a2} is most likely also related to the high electron concentration in the accumulated region. When the current density in CeO_2 increases, the number of occupied energy states in the conduction band increases. Hence it is assumed that the activation energy E_a from the trap level to the first free electron state in the conduction band should increase with increasing electron density.

4. Conclusions

The fabrication and characterization of the Pt/*n*-Si/CeO_2/Pt MOS capacitor structure were described. The electrical properties of the CeO_2 thin films were characterized by examining and modelling the C-V response of the MOS structure utilizing impedance spectroscopy. The CeO_2 layer was found to have a dielectric constant of $\varepsilon_r = 22$. The dielectric constant ε_r and loss angle tan δ had space charge polarization type dependence at frequencies below 100 Hz. The *dc*-conductivity was also found to be three orders of magnitude higher for randomly oriented nanocrystalline films with activation energy $E_a = 0.45$ eV in comparison with columnar oriented films. This was contributed to the increased electron density in the CeO_2 grains due to cation impurity segregation to the high volume fraction grain boundaries. Above a certain positive gate bias, there was an increase in the value of the oxide capacitance C_{ox}, likely due to the depletion inside the CeO_2 thin film and the generation of accumulated space charge capacitance C_a. Subsequently, the small polaron bulk hopping conductivity response changed to Schottky emission and tunneling in the depleted region, and thermally activated hopping conduction in the accumulated region with $E_a = 0.53$ eV.

Acknowledgments

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